Patent USSR SU 1332312

Dividing Device

Application no.: 3867061 / 24 – 24
Application date: March, 05, 1985
Publication date: August, 23, 1987, Bulletin Izobretenii no. 31
Applicant: Minsk Radio-Engineering Institute
Inventors: Alexander Nozik and Alexander Shostak
Classification: G 06 F 7/52

***Abstract* — This invention is related to the area of computing machinery and can be used to perform the division procedure. The invention allows for a significant increase in the performance of the existing device. The device consists of the multipliers, the adders, and the subtractors forming a triangular cellular array, and the converter of the redundant binary code to the non-redundant binary code.**

This invention is related to the area of computing machinery and can be used to perform the division procedure.

The purpose of the invention is to increase the performance of the existing division device.

Fig. 1 provides the internal structure of the device; Fig. 2, Fig. 3, and Fig. 4 provide the functional charts of the multiplier, adder, and subtractor respectively; Fig. 5 provides the internal structure of the converter of the redundant binary code to the non-redundant binary code.

The division device is a triangle array consisting of a total of 21 multipliers numbered 1, a total of 17 adders numbered 2, a total of 13 subtractors numbered 3, and a converter 4 for converting the redundant binary code to the non-redundant binary code.

< The description of the connectivity of the appropriate blocks is skipped >

The division device is based on the following idea. Assume that the dividend $C = 0.\ c_1\ c_2\ c_3\ c_4\ c_5\ c_6\ c_7\ c_8$ and the divisor $A = 0.\ a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8$ are normalized positive binary fractions and the quotient Q is represented as follows:

$$Q = C / A = q_0 \,.\, q_1\, q_2\, q_3\, q_4\, q_5\, q_6\, q_7\,,$$

where q_i is ith redundant quotient digit and $0 \le i \le 7$.
The condition $A \cdot Q = C$ can be used to determine the redundant quotient digits by assigning the sums of the partial products with equal binary weights to the corresponding digits of the dividend C. The dividend C is represented in the device in the following form:

$$C = 0.\, c_1c_2c_3c_4c_5c_6c_7c_8 = c_1 \cdot 2^{-1} + c_2 \cdot 2^{-2} + 0 \cdot 2^{-3} + (2c_3 + c_4) \cdot 2^{-4} + 0 \cdot 2^{-5} + (2c_5 + c_6) \cdot 2^{-6} + 0 \cdot 2^{-7} + (2c_7 + c_8) \cdot 2^{-8}.$$

As a result, the following system of linear equations can be obtained:

$$\begin{aligned}
&a_1q_0 = c_1 \\
&a_1q_1 + a_2q_0 = c_2 \\
&a_1q_2 + a_2q_1 + a_3q_0 = 0 \\
&a_1q_3 + a_2q_2 + a_3q_1 + a_4q_0 = 2c_3 + c_4 \\
&a_1q_4 + a_2q_3 + a_3q_2 + a_4q_1 + a_5q_0 = 0 \\
&a_1q_5 + a_2q_4 + a_3q_3 + a_4q_2 + a_5q_1 + a_6q_0 = 2c_5 + c_6 \\
&a_1q_6 + a_2q_5 + a_3q_4 + a_4q_3 + a_5q_2 + a_6q_1 + a_7q_0 = 0 \\
&a_1q_7 + a_2q_6 + a_3q_5 + a_4q_4 + a_5q_3 + a_6q_2 + a_7q_1 + a_8q_0 = 2c_7 + c_8
\end{aligned} \qquad (1)$$

Taking into account the fact that A and C are normalized binary fractions i.e. $a_1 = c_1 = 1$, equations (1) can be rewritten as follows:

$$\begin{aligned}
&q_0 = 1 \\
&q_1 = c_2 - a_2 \\
&q_2 = -a_2q_1 - a_3 \\
&q_3 = 2c_3 + c_4 - a_2q_2 - a_3q_1 - a_4 \\
&q_4 = -a_2q_3 - a_3q_2 - a_4q_1 - a_5 \\
&q_5 = 2c_5 + c_6 - a_2q_4 - a_3q_3 - a_4q_2 - a_5q_1 - a_6 \\
&q_6 = -a_2q_5 - a_3q_4 - a_4q_3 - a_5q_2 - a_6q_1 - a_7 \\
&q_7 = 2c_7 + c_8 - a_2q_6 - a_3q_5 - a_4q_4 - a_5q_3 - a_6q_2 - a_7q_1 - a_8
\end{aligned} \qquad (2)$$

The equations (2) can be transformed by substituing the expression for q_2 from the third equation of (2) to the expression for q_3 in the fourth equation of (2). In a similar way, the expression for q_3 from the fourth equation of (2) can be substituted into the expression for q_4 in the fifth equation of (2) and so on. The resulting expressions for the redundant digits q_i $(0 \le i \le 7)$ of the quotient are as follows:

$q_0 = 1$
$q_1 = c_2 - a_2$
$q_2 = -a_3 - a_2q_1$
$q_3 = 2c_3 + c_4 - a_4 - a_3q_1 - a_2(-a_3 - a_2q_1)$
$q_4 = -a_5 - a_4q_1 - a_3q_2 - a_2(2c_3 + c_4 - a_4 - a_3q_1 - a_2q_2)$
$q_5 = 2c_5 + c_6 - a_6 - a_5q_1 - a_4q_2 - a_3q_3 - a_2(-a_5 - a_4q_1 - a_3q_2 - a_2q_3)$
$q_6 = -a_7 - a_6q_1 - a_5q_2 - a_4q_3 - a_3q_4 - a_2(2c_5 + c_6 - a_6 - a_5q_1 - a_4q_2 - a_3q_3 - a_2q_4)$
$q_7 = 2c_7 + c_8 - a_8 - a_7q_1 - a_6q_2 - a_5q_3 - a_4q_4 - a_3q_5 - a_2(-a_7 - a_6q_1 - a_5q_2 - a_4q_3 - a_3q_4 - a_2q_5)$

(3)

Taking into account the fact that a_2 is a binary variable that can assume only the values of either 0 or 1, and that the expression $a_2 \cdot a_2 = a_2$, the expressions in parentheses in the right side of the equations (3) can be simplified. For instance, the expression $a_2(-a_3 - a_2q_1)$ in the right side of the the fourth equation of (3) can be converted to the following form:

$$a_2(-a_3 - a_2q_1) = -a_2a_3 - a_2a_2q_1 = -a_2a_3 - a_2q_1 = a_2(-a_3 - q_1).$$

After performing the similar conversion for the fifth, sixth, seventh, and the eighth equations, the equations (3) for calculations of the redundant digits q_i $(0 \le i \le 7)$ will be as follows:

$q_0 = 1$
$q_1 = c_2 - a_2$
$q_2 = -a_3 - a_2q_1$
$q_3 = 2c_3 + c_4 - a_4 - a_3q_1 + a_2(a_3 + q_1)$
$q_4 = -a_5 - a_4q_1 - a_3q_2 - a_2(2c_3 + c_4 - a_4 - a_3q_1 - q_2)$
$q_5 = 2c_5 + c_6 - a_6 - a_5q_1 - a_4q_2 - a_3q_3 + a_2(a_5 + a_4q_1 + a_3q_2 + q_3)$
$q_6 = -a_7 - a_6q_1 - a_5q_2 - a_4q_3 - a_3q_4 - a_2(2c_5 + c_6 - a_6 - a_5q_1 - a_4q_2 - a_3q_3 - q_4)$
$q_7 = 2c_7 + c_8 - a_8 - a_7q_1 - a_6q_2 - a_5q_3 - a_4q_4 - a_3q_5 + a_2(a_7 + a_6q_1 + a_5q_2 + a_4q_3 + a_3q_4 + q_5)$.

(4)

The device (Fig.1) forms the redundant digits of the quotient according to the equations (4). For instance, the redundant digit q_1 is formed by the output of the subtractor 3 in the first row of the first column of the triangle matrix. The first input of subtractor 3 is connected to the input 6_1 of the device which is used to provide the digit c_2 of the dividend C. The second input of the subtractor 3 is connected to the first input of the group of inputs 5 which is used to provide the digit a_2 of the divider A. The redundant digit q_2 is formed as follows. The multiplier 1 in the second row of the first column of the triangle matrix forms the value of a_2q_1 which is supplied to the first input of the adder 2 of the same column and of the same row of the matrix. The second input of the adder 2 is connected to the value a_3 of the divisor A which is supplied from the input 5_2 of the device. Therefore, the adder 2 produces the value of $a_3 + a_2q_1$ which is equal to the

value q_2 from the third equation of (4) but with the opposite sign. The resulting value $-q_2$ is supplied to the corresponding input of the block 4 where that value of $-q_2$ is added to the rest of the redundant quotient digits taking into account the sign of $-q_2$.

The digit q_3 is formed by the output of the adder 2 in the third row of the first column of the matrix accoridng to the following algorithm. The multiplier 1 in the second column of the second row of the matrix formulates the value a_3q_1 which is provided to the first input of the subtractor 3 of the same column and of the same row of the matrix. The second input of that subtractor 3 is connected to the output of the subtractor 3 in the first row of the third column of the matrix which forms the value $2c_3 + c_4 - a_4$ by subtracting the value of a_4 on the input 5_3 from the value of $2c_3 + c_4$ provided on the inputs 6_2 and 6_3 of the device.

The output of the subtractor 3 in the second row of the second column of the matrix forms the value of $2c_3 + c_4 - a_4 - a_3q_1$ which is provided to the second input of the adder 2 in the third row of the first column of the matrix. The value of $a_2\ (a_3+q_1\ )$ is provided to the first input of the same adder from the output of the corresponding multiplier 1, the first input of which is connected with the input 5_1 of the device and the second input of which is connected to the output of the adder 2 in the second row of the second column of the triangle matrix. The first input of that adder is connected with the output of the subtractor 3 in the first row of the first column of the triangle matrix which provides the value of q_1, and the second input of that adder is connected with the input 5_2 of the device which provides the value of a_3 of the divisor *A*. Therefore, the output of the adder 2 of the third row and of the first column forms the value of $q_3 = 2c_3 + c_4 - a_4 - a_3q_1 + a_2\,(a_3 + q_1\ )$.

The quotient digit q_4 is formed (with the opposite sign) on the output of the adder 2 in the fourth row of the first coulmn of the matrix as follows. The output of the adder 2 in the second row of the third column of the matrix forms the value of $a_4q_1 + a_5$ by adding the value of a_5 of divisor *A* provided by the input 5_4 of the device with the value of a_4q_1 provided by the output of the multiplier 1 in the second row of the third column of the matix. The value of $a_4q_1 + a_5$ from the output of the corresponding adder 2 is provided to the first input of the subtractor 3 in the third row of the second column of the matrix. The second input of the subtractor is connected with the output of the multiplier 1 in the third row of the second column of the matrix which provides the value of $-q_2a_3$. The resulting value of $a_4q_1 + a_5 + a_3$ which is formed on the output of the corresponding subtractor *3* is supplied to the second input of the adder *2* in the fourth row of the first column of the matrix. The value of $a_2\ (2c_3 + c_4 - a_4 - a_3q_1 - q_2\ )$ is provided to the first input of the adder 2 in the fourth row of the first column of the matrix. It is formed on the output of the multiplier *1* in the fourth row of the first column of the matrix, the first input of which is connected with the input 5_1 of the device and the second input of which is connected with the output of the adder *2* in the third row of the second column of the matrix which forms the value of $2c_3 + c_4 - a_4 - a_3q_1 - q_2$. Thus, the output of the adder 2 in the fourth row of the first column forms the value of $-q_4 = a_5 + a_4q_1 + a_3q_2 + a_2\,(2c_3 + c_4 - a_4 - a_3q_1 - q_2)$ which differs from the value of q_4 from the equations (4) only by its sign.

The remaining quotient redundant digits q_5, q_6, and q_7, are formed similarily. It has to be noted that the values of the redundant digits q_2, q_4, and q_6 are formed with the opposite signs by the device. This fact is taken into the account by the block *4* which

converts the quotient from the redundant form into the non-redundant binary form. The value of q_0 is always equal to 1 and therefore it is not formed explicitly by the device. However, the value of $q_0 = 1$ is taken into account in block 4 while forming the value of the quotient in the non-redundant binary form $Q = q_0^*.\ q_1^*\ q_2^*\ q_3^*\ q_4^*\ q_5^*\ q_6^*\ q_7^*$ on the outputs 7_1 - 7_8 of the device.

The following table provides the maximum and the minimum possible values of the redundant quotient digits for the proposed device.

Maximum and minimum values of the redundant quotient digits	Redundant quotient digits						
	q_1	q_2	q_3	q_4	q_5	q_6	q_7
q_{min}	*1*	*1*	*4*	*3*	*7*	*8*	*13*
q_{max}	*-1*	*-1*	*-2*	*-5*	*-5*	*-9*	*-13*

It should be noted that if the number of digits of the divider and the dividend is odd (for instance, $n=p=7$), then the dividend C is represented as follows:

$$C = 0.\ c_1c_2c_3c_4c_5c_6c_7c_8 = c_1\cdot 2^{-1} + c_2\cdot 2^{-2} + 0\cdot 2^{-3} + (2c_3+c_4)\cdot 2^{-4} + 0\cdot 2^{-5} + \\ + (2c_5+c_6)\cdot 2^{-6} + c_7\cdot 2^{-7}.$$

This affects the expression for q_6 which in that case will be as follows:

$$q_6 = c_7 - a_7 - a_6q_1 - a_5q_2 - a_4q_3 - a_3q_4 - a_2\,(2c_5 + c_6 - a_6 - a_5q_1 - a_4q_2 - a_3q_3 - q_4)$$

Consider the implementation of the division device using as an example multiplier 1 and adder 2 in the fourth row of the first column, and the subtractor 3 in the first row of the third column, and the converter 4 for converting the redundant binary code into the non-redundant binary code. Here and onwards we assume that the redundant quotient digits are represented in two's complement code. In case the redundant quotient digits are represented in one's complement code, the implementation of some blocks might be slightly different.

Multiplier 1 is used to form the value of $a_2\,(2c_3 + c_4 - a_4 - a_3q_1 - q_2)$ which according to the third equation of (2) is equal to the result of the multiplication of q_3 and $a_{2..}$ Since according to the table above $q_3^{min} = -2$ and $q_3^{max} = 4$, the multiplier 1 can be implemented using four two-input AND elements $8_1 - 8_4$ (Fig. 2). The element 8_1 is used to form the sign of the multiplication result.

Adder 2 performs the summation of the results which are formed on the output of the multiplier 1 in the fourth row of the first column and on the output of the subtractor 3 in the third row of the second column. The output of the adder 2 forms the value $-q_4$ which has the maximum absolute value equal to 5 (according to the table above). This adder can be implemented using four single-bit full binary adders $9_1 - 9_4$. (Fig.3). The adder 9_1 is used to form the sign of the result.

Subtractor 3 performs the calculation of the value of $2c_3 + c_4 - a_4$. It consists of two single-bit binary subtractors 10_1 and 10_2 (Fig.4). The "borrow" output of subtractor 10_1 represents the "sign" of the calculated value of $2c_3 + c_4 - a_4$.

Block 4 performs the conversion of the quotient from the redundant binary form represented as a set of the redundant binary digits q_i $(0 \le i \le 7)$ into the non-redundant binary form taking into account the fact that digits q_2 , q_4, and q_6 , are formed with the opposite signs. The simplified diagram of block 4 is presented in Fig. 5. This block consists of converters 11_1 - 11_3 that perform the sign conversion of the redundant quotient digits $-q_2$, $-q_4$, and $-q_6$. It also consists of block 12 of for converting "eight-row" binary code into the "two-row" binary code and the carry look-ahead adder 13. The converters 11_1 - 11_3 actually perform the logical inversion of the input code , i.e. they perform the "one's complement" conversion of the input code. The further conversion of the $-q_2$, $-q_4$, and $-q_6$ into the "two's complement" code is performed in block 12 by providing the proper "1" signals on the carry inputs of the corresponding single-bit adders of block 12. In general, block 12 performs the multi-operand algebraic binary addition of the input binary signals according to its binary weights and the carry look-ahead adder forms the quotient in the non-redundant binary form.

The device operates according to the following algorithm. The values of the binary digits of divider $C = 0.\ c_1\ c_2\ c_3\ c_4\ c_5\ c_6\ c_7\ c_8$ and the divisor $A = 0.\ a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8$ are provided to the inputs 6_1 - 6_7 and 5_1 - 5_7 of the device. (The values of $c_1 = 1$ and $a_1 = 1$ are not used as explicit input values). Then the device sequentially forms the values of the redundant quotient digits $q_1, -q_2, q_3, -q_4, q_5, -q_6, q_7$ according to (4). The value of q_7 will be formed in approximately $4t_m + 7t_a$ where t_m – is the delay of multiplier 1 and t_a is the delay of adder 2 (and subtractor 3). The formed values of the redundant quotient digits are provided to the inputs of block 4 that converts it into the non-redundat binary code $Q = q_0^*.\ q_1^*\ q_2^*\ q_3^*\ q_4^*\ q_5^*\ q_6^*\ q_7^*$. The total time of forming the quotient into the non-redundant binary form is $4t_m + 7t_a + t_{conv}$ where t_{conv} is the delay of block 4. It should be noted that the process of conversion of the quotient in block 4 overlaps with the process of forming the redunant quotient digits. In general, the time T_p required to form the p quotient digits in the suggested device for even values of p can be defined using the following expression:

$$T_p \approx (p-1)\ t_a + (p/2)\ t_m + t_{conv}$$